Abstract of the Disclosure

In a method and system for cycling through addresses of a memory device, a respective bit pattern comprised of a predetermined number of bits is generated for each address. The respective bit pattern for each of the addresses is cycled through with a transition of less than the predetermined number of bits for sequencing to each subsequent address. For example, the respective bit pattern for each of the addresses is cycled through in a gray code sequence. By limiting the number of transitions in the address bits, charge gain failure of a flash memory device is minimized and even may be eliminated.